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	Application No.	Applicant(s)		
Al-C A All-wall Wes	10/652,635 SI			
Notice of Allowability	Examin r	Art Unit		
	Lisa Kilday	2829		
The MAILING DATE f this c mmunication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.				
1. This communication is responsive to <u>8/28/03</u> .				
2. The allowed claim(s) is/are <u>1-22</u> .				
3. The drawings filed on 28 August 2003 are accepted by the Examiner.				
4.				
 Attachment(s) 1. Notice of References Cited (PTO-892) 2. Notice of Draftperson's Patent Drawing Review (PTO-948) 3. Information Disclosure Statements (PTO-1449 or PTO/SB/O Paper No./Mail Date	5. ☐ Notice of Informal P 6. ☐ Interview Summary Paper No./Mail Dat 7. ☐ Examiner's Amendn 8. ☑ Examiner's Stateme 9. ☐ Other	(PTO-413), e nent/Comment		

Allowable Subject Matter

Claims 1-22 allowed.

The following is an examiner's statement of reasons for allowance: Chung et al. (US 2003/0064598) teaches in fig. 1-8 a process for filling a trench of a semiconductor device, the method comprising: providing a semiconductor substrate (10); forming a silicon nitride layer (26) on said semiconductor substrate; forming an oxide layer (24); partially removing said oxide layer, said silicon nitride layer and said semiconductor substrate to form at least one trench (ref. 12, 14); and forming a trench-fill layer (40) to fill said trench (¶¶16, 19, 40). Chung et al. teaches forming a sidewall layer of silicon nitride (ref. 36), however Chung et al. does not teach removing the sidewall layer of silicon nitride that *protrudes* from the sidewall of the trench. Prior art does not teach or suggest forming a trench in an oxide layer, silicon nitride layer, and semiconductor substrate in combination with the limitation of performing an etching procedure to remove portions of said silicon nitride layer *protruding from said sidewalls* in order to form substantially even sidewalls of said trench.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chau et al. (5,244,843) teaches a method of forming a sacrificial

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oxide layer and removing the sacrificial oxide layer (abstract; col. 1, lines 30-56; col. 2, lines 26-30; ref. 25); Lin et al. (US 2003/0216044) teaches a method of forming a Silicon oxide bottle trench; and Lin et al. (US 2004/0082200) teaches a method of forming a Silicon nitride bottle trench (ref. 260a, 260b).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0957. See MPEP 203.08.

Any inquiry concerning this communication from the examiner should be directed to Lisa Kilday whose telephone number is (571) 272-1962. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo, can be reached on (571) 272-1957. The fax number for the group is (703) 872-9306. MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

Lisa Kilday

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6/12/04

KAMAND CUNEO

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